ABSTRACT OF THE DISCLOSURE

A plurality of dummy bit lines are disposed together with a plurality of bit line pairs in a memory cell array. In selectively driving a memory cell connected to the bit line pair, a timing control circuit controls the timing of the driving operation, based on signal change in the plural dummy bit lines, thereby detecting the influences of the process variation in a plurality of positions in the memory cell array. Thus, the influence of the process variation given to the operation of a semiconductor memory device can be further alleviated, compared with the case when one dummy bit line is used.